K-Band Circulators on Semiconductor Wafers

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ABSTRACT

We report on the development of K-band circulators operating at 20 and 35 GHz which have been monolithically integrated with both GaAs and epitaxial GaAs-on-Si wafers. They demonstrate the potential for a fully integrated T/R module application.

INTRODUCTION

Previously[1] we noted that cost and size reductions for T/R module applications were the drivers for integrating passive components (circulators) with GaAs MMICs. The challenge of bonding dissimilar materials with different coefficients of thermal expansion, and protecting the GaAs from the high temperatures of the ferrite film fabrication process, have been tackled with degrees of success. Reference (1) showed results for an X-band circulator on a Si wafer.

This circulator required two stages of matching plus a tab extension at its ports on the Yttrium Iron Garnet (YIG) disc and resulted in a diameter of 14 mm. For phased array applications, this represents a fair amount of "real estate" in a T/R module element. There are advantages in going to higher frequencies. (1) For a given ferrite thickness, the circulator port impedance increases with frequency while the circulator diameter decreases with frequency. Figure 1 shows these results calculated for a YIG disc 0.1 mm thick. (2) The maximum substrate thickness before radiation from a lowest order surface wave mode becomes significant[2] as a function of frequency lies above the curve of circulator thickness with a 50 Ohm port impedance at K-band frequencies and higher. Figure 2 shows these calculated results for YIG.

RESULTS

Our technique for ferrite film deposition on to semiconductor wafers is pulsed laser deposition (PLD)[3]. K-band circulators were grown on 3" diameter liquid encapsulated Czochralski grown semi-insulating GaAs substrates. A barrier layer is needed to prevent the escape of arsenic during the PLD process and a sputtered double layer of SiO_2 and Si_3N_4 was suggested to us [4]. On the barrier layer a 3 micron Au ground plane was evaporated. This served two functions: (a) the ground plane for the circulators and the active circuits (FETs); (b) a stress relief material which bonded the ferrite to the substrate.

100 microns of YIG was deposited through a shadow mask using the PLD process. Occasionally the GaAs substrate would fracture, and this prompted us to use the mechanically stronger Si wafers as a second choice. These were 3" diameter float zone material with a resistivity >10 kΩ cm. An epi-GaAs layer, about 0.5 micron thick, was deposited by MOCVD using a standard two step procedure. Then followed the barrier layer and Au ground plane. Figure 3

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shows a GaAs-on-Si wafer with 20 and 35 GHz circulators and

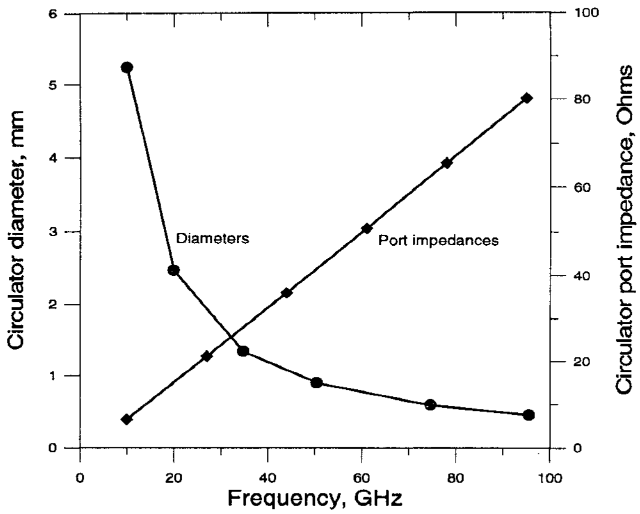

Fig. 1. The calculated circulator diameter and port impedance as a function of frequency for 0.1 mm thick YIG.

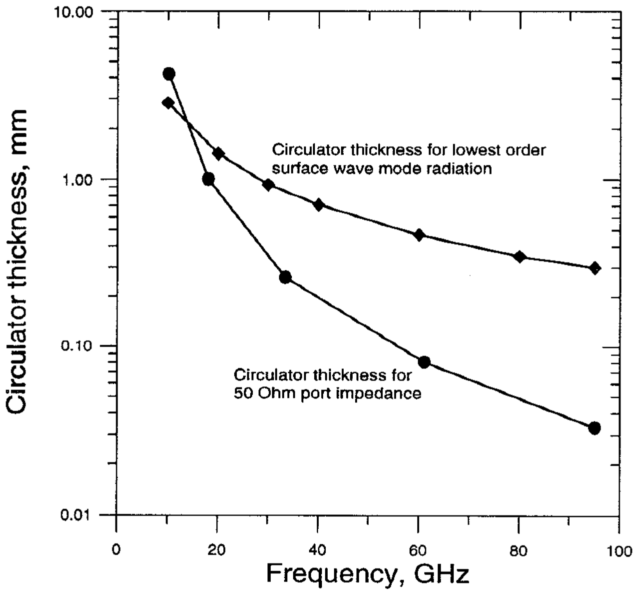

Fig. 2 Upper curve: The calculated YIG sustrate thickness for the lowest order surface wave radiation mode as a function of frequency. Lower curve: The calculated YIG thickness for a 50 Ohm port impedance circulator as a function of frequency.

test matching sections.Two options were taken with the top metalization. In one case the 50 Ohm microstrip line extends to the edge of the YIG disc and then transitions down the sloping edge of the YIG to a 50 Ohm CPW formed as part of the ground plane circles. In the second option the 50 Ohm microstrip transitions to a short section of 50 Ohm CPW for contact with a wafer probe within the diameter of the YIG disc. In this geometry, the ground plane sections of the CPW transition down the YIG disc edge to contact the ground plane circles.

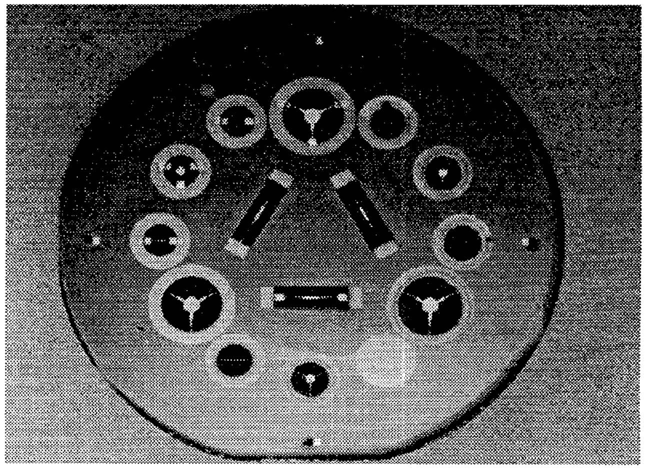

Fig. 3. Photograph of a completed GaAs-on-Si wafer showing 20 and 35 GHz circulators on gold ground planes along with test matching sections.

The circulator and matching section designs were based on Neidert and Phillips[5] and incorporated into HP's DCS software as a circuit element.

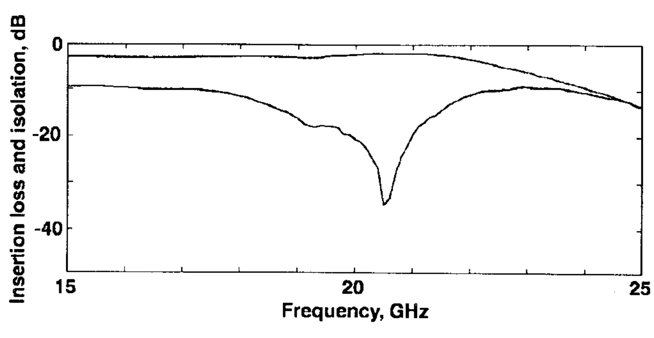

Fig. 4. The insertion loss and isolation of a 20 GHz circulator as a function of frequency.

Magnetic biasing of a circulator was done with a Nd-Fe-B magnet. This was placed above a circulator with a soft iron plate below the semiconductor substrate.Thus the magnet flux was directed down through the circulator and normal to its plane.

The results of network analyzer measurements on a 20 and 35 GHz device are respectively shown in figures 4 and 5. In both devices the isolation is good, however, additional studies are being made to determine why the insertion losses are in excess of 1 dB, particularly for the results at 35 GHz. Attention is focused on possible dielectric losses.

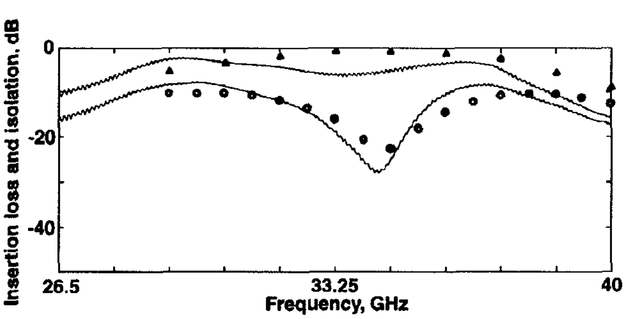

Fig. 5. The insertion loss and isolation of a 35 GHz circulator as a function of frequency. The triangles and circles are respectively the calculated insertion loss and isolation.

Work is presently in hand to fabricate the sub-micron gate FETs for the active part of the devices. These will be written by e-beam lithography.

ACKNOWLEDGMENT

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